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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Cheah, Eng-Chew	Confirmation No. 1049
Serial No. 09/863,652	Examiner: David A. Zarneke
Filed: May 22, 2001	Group Art Unit: 2829
Title: MULTI-TIERED LEAD PACKAGE FOR AN INTEGRATED CIRCUIT	Attorney Docket No. 060889-0050-US

APPEAL BRIEF

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Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

(i) Real party in interest

The real party in interest is Altera Corporation, 101 Innovation Drive, San Jose, California.

(ii) Related appeals and interferences

There are no related appeals and interferences.

(iii) Status of claims

Claims 9-13 have been rejected and their rejection is being appealed. Claims 1-8 and 14- have been canceled.

(iv) Status of amendments

No amendment was filed subsequent to the close of prosecution.

(v) Summary of claimed subject matter

Independent claim 9 is directed to a semiconductor package (100; Specification, page 3, line 27) that includes an intermediate lead finger mounting substrate (120; page 3, line 31 to page 4, line 1). A semiconductor die (130; page 4, line 6) and an intermediate lead finger (125a-125d: page 4, lines 7-8) are mounted on a first surface of the intermediate lead finger mounting substrate (120). The package further

includes a package lead (150; page 4, line 10) and a bond wire (140; page 4, line 15) having a first end coupled to the package lead (page 4, lines 15-16), a second end coupled to a bond pad (135; page 4, line 16) on the die and an intermediate portion. The intermediate lead finger is positioned between the package lead and the bond pad and is attached to the intermediate portion of the bond wire (page 4, lines 17-18) and remains so attached through a subsequent molding process. The package further includes a heat sink (110; page 3, line 31) coupled to the second surface of the mounting substrate and a molding compound (page 4, lines 21-23) enclosing the die, a portion of the package lead, the bond wire, the intermediate lead finger and the heat sink.

(vi) Issues to be reviewed on appeal

Whether claims 9-13 are properly rejected under 35 U.S.C. 103(a) as unpatentable over Aoki et al., U.S. Patent No. 4,903,114 in view of Gainey et al., U.S. Patent No. 6,313,519, and Lacap, U.S. Patent No. 5,905,299?

(vii) Argument

Aoki et al. describes in Fig. 7 a semiconductor package in which a first bond wire 18 runs from a chip pad 511 to a relay pad 13 and a second bond wire 19 runs from the relay pad to inner leads 5. Gainey et al. shows a continuous bond wire attached to a die and a lead finger and bonded to a support structure at an intermediate point.

In rejecting claim 9, the Examiner acknowledges that his primary reference, Aoki et al., does not disclose the use of a single bond wire running from the die to the package lead but relies on Gainey for such teaching. He also acknowledges that both Aoki and Gainey fail to teach a heat sink coupled to the second surface of an intermediate lead finger mounting substrate and the use of a mold compound but asserts that Lacap provides such teaching.

While Lacap does disclose the use of heat sink (614), he does not disclose the use of a heat sink on a side of an intermediate lead finger mounting substrate different from the side on which the semiconductor die is mounted. Indeed, Lacap does not disclose the use of any means for securing lead fingers at an intermediate point and, in particular, does not disclose the use of an intermediate lead finger mounting substrate.

Since Lacap does not disclose the use of an intermediate lead finger mounting substrate, he also does not suggest the specific structure claimed in claim 9 in which

the heat sink is on a first side of the intermediate lead finger mounting substrate and the semiconductor die is on a second side.

Since Lacap is concerned with improving the thermal performance of flatpack packages while Gainey and Aoki are concerned with supporting lead wires, there is also no suggestion in these references that the references be combined. Lacap simply does not mention the need for improving support for semiconductor bond wires and Aoki and Gainey do not address thermal performance issues. In the absence of any mention in one reference of the problems addressed by the other reference(s), there is simply no suggestion that the references be combined and no motivation to combine them.

In the Office Action of April 27, 2005, the Examiner took the position that the reason to combine references need not be found in the references, citing the first paragraph of MPEP 2144. As is well known, however, the MPEP is not controlling precedent. Moreover, in arguing this way instead of pointing to any suggestion in the references for their combination, the Examiner concedes that no suggestion for their combination can be found in the references. Applicants respectfully disagree both with the Examiner's reliance on the MPEP and with its application to the present circumstances.

The Examiner's argument is an argument from hindsight. He has taken the elements of applicants' claim 9, located them in the prior art and asserted that these elements can be combined even though there is no suggestion in the cited prior art for their combination. The Examiner's schema of argument is expressly prohibited in numerous decisions of the Federal Circuit. For example, in Heidelberger Druckmaschinen AG v. Hantscho Commercial Products, Inc., 21 F. 3d 1068, 30 USPQ 2d 1344 (Fed. Cir. 1993), the Federal Circuit warned:

> "When the patented invention is made by combining known components to achieve a new system, the prior art must provide a suggestion or motivation to make such a combination." (emphasis supplied) 30 USPQ 2d at 1379.

Moreover, to prevent such hindsight arguments, the Federal Circuit has also required that there must not only be motivation to combine references but also motivation to combine the prior art teachings in the particular manner claimed:

> "particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed." In re Kotzab, 217 F. 3d 1365, 1371, 55 U.S.P.Q. 2d 1313, 1317 (Fed. Cir. 2000).

The Examiner concedes that the suggestion to combine these references is not to be found in the references. Neither is there any motivation to combine these references in the manner claimed. The Gainey and Aoki references make no mention of thermal issues. The Lacap reference makes no mention of packages that use intermediate lead fingers that are attached to intermediate portions of bond wires. As a result, there is no motivation in Gainey or in Aoki to add a heat sink of any sort to the packages they disclose and there is no motivation in Lacap to add an intermediate lead finger to the structures he discloses.

The Examiner argues instead that heat sinks are widely used, but merely to argue that heat sinks are widely used does not establish that there is any need to use them with intermediate lead fingers of the type disclosed by Gainey and Aoki and it does not establish that one skilled in the art would combine the elements of the cited references in the manner claimed by applicants.

For these reasons, it is respectfully submitted that claim 9 is patentable over the cited references.

Dependent claims 10-13 are patentable for the same reason claim 9 is patentable.

Respectfully submitted,

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(viii) Claims Appendix

The claims to be reviewed on appeal are as follows:

9. (Previously Presented) A semiconductor package, comprising:

an intermediate lead finger mounting substrate having a first surface and a second surface;

a semiconductor die with a bond pad, the semiconductor die being attached on the first surface of the intermediate lead finger mounting substrate;

a package lead;

a bond wire comprising a first end portion coupled to the package lead, a second end portion coupled to the bond pad, and an intermediate portion;

an intermediate lead finger mounted on the first surface of the intermediate lead finger mounting substrate, wherein the intermediate lead finger is positioned between the package lead and the bond pad, and wherein the intermediate lead finger is attached to the intermediate portion of the bond wire, and remains so attached through a subsequent molding process;

a heat sink coupled to the second surface of the intermediate lead finger mounting substrate; and

a mold compound that encloses the semiconductor die, a portion of the package lead, the bond wire, the intermediate lead finger, and the heat sink.

10. (Previously Presented) The package of claim 9, wherein the intermediate lead finger and the intermediate lead finger mounting substrate are formed of a non-conducting material.

11. (Previously Presented) The package of claim 9, wherein the intermediate lead finger comprises a non-conducting portion for attaching to the intermediate portion of the bond wire.

12. (Previously Presented) The package of claim 9, wherein the semiconductor die comprises a programmable logic device.

13. (Previously Presented) The package of claim 9, wherein the semiconductor die is mounted on a center portion of the first surface of the intermediate lead finger mounting substrate, and wherein the intermediate lead finger is mounted on a peripheral portion of the first surface of the intermediate lead finger mounting substrate.